outward from substrate [212] <u>201</u> of, for example, p- silicon. First source/drain region 206 and second source/drain region 210 each comprise, for example, n+ silicon and body region 208 comprises p- silicon

The paragraph beginning at page 10, line 13 is amended as follows:

Memory cell 202C also includes storage capacitor 219 for storing data in the cell. A first plate of capacitor 219 for memory cell 202C is integral with second source/drain region 210 of access transistor 211. Thus, memory cell 202C may be more easily realizable when compared to conventional vertical transistors since there is no need for a contact between second source/drain region 210 and capacitor 219. Second plate 220 of capacitor 219 is common to all of the capacitors of array 200. Second plate 220 comprises a mesh or grid of n+ poly-silicon formed in deep trenches that surrounds at least a portion of second source/drain region 210 of each pillar 204A through 204D. Second plate 220 is grounded by contact with substrate [212] <u>201</u> underneath the trenches. Second plate 220 is separated from source/drain region 210 by gate oxide 222.

The paragraph beginning at page 11, line 22 is amended as follows:

As shown in FIG. 5A, the method begins with substrate 300. Substrate 300 comprises, for example, a P-type silicon wafer, layer of P- silicon material, or other appropriate substrate material. <u>As shown in FIG. 5A, substrate 300 is a single unbonded substrate.</u> Layer 302 is formed, for example, by epitaxial growth outwardly from layer 300. Layer 302 comprises single crystalline N+ silicon that is approximately 3.5 micrometers thick. Layer 304 is formed outwardly from layer 302 by epitaxial growth of single crystalline P- silicon of approximately 0.5 microns. Layer 306 is formed by ion implantation of donor dopant into layer 304 such that layer 306 comprises single crystalline N+ silicon with a depth of approximately 0.1 microns.